

Application No.: 10/549,291

REMARKS

Claims 1-4, 6-8, and 12-22 are pending in this application, with claims 1, 6, and 14 being independent. Claims 1 and 6 have been amended. Claims 14-22 have been added. Claims 9-11 have been canceled without prejudice and/or disclaimer of the subject matter. Favorable reconsideration of the application in light of the following comments is respectfully solicited.

Claim Rejections – 35 U.S.C. § 103

Claims 1, 2, 4, and 12 were rejected under 35 U.S.C. § 103(a) as being obvious by U.S. Patent Number 6,288,431 (“Iwasa”) in view of U.S. Patent Number 4,996,574 (“Shirasaki”). This rejection is traversed for at least the following reasons.

As amended, claim 1 recites a semiconductor device that includes, among other features, a semiconductor substrate in which a trench is formed, the semiconductor substrate contains an impurity of a first conductive type. The semiconductor device also includes a source region and a drain region, each of which is buried in the trench and contains an impurity of a second conductive type. Additionally, the semiconductor device includes a channel stopper formed in a region located at a bottom portion of the trench in the semiconductor substrate and containing an impurity of the first conductive type at a higher concentration than that in the semiconductor substrate.

Applicants respectfully submit that Iwasa and Shirasaki, either alone or in combination, fail to describe or suggest a semiconductor device that includes, among other features, a semiconductor substrate in which a trench is formed, the semiconductor substrate contains an impurity of a first conductive type; a source region and a drain region, each of which is buried in the trench and contains an impurity of a second conductive type; and a channel stopper formed in

Application No.: 10/549,291

a region located at a bottom portion of the trench in the semiconductor substrate and containing an impurity of the first conductive type at a higher concentration than that in the semiconductor substrate, as recited in claim 1 (emphasis added).

For at least this reason, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 1.

As amended, claim 6 recites a semiconductor device that includes, among other features, a first field-effect transistor including a semiconductor substrate having a trench formed therein and containing an impurity of a first conductive type. The semiconductor device also includes a first source region and a first drain region each of which is buried in the trench and contains an impurity of a second conductive type. Additionally, the semiconductor device includes a channel stopper formed in a region located at the bottom of the trench in the semiconductor substrate and containing an impurity of the first conductive type at a higher concentration than that in the semiconductor substrate.

Applicants respectfully submit that Iwasa and Shirasaki, either alone or in combination, fail to describe or suggest a semiconductor device that includes, among other features, a first field-effect transistor including a semiconductor substrate in which a trench is formed and containing an impurity of a first conductive type, a first source region and a first drain region each of which is buried in the trench and contains an impurity of a second conductive type, and a channel stopper formed in a region located at the bottom of the trench in the semiconductor substrate and containing an impurity of the first conductive type at a higher concentration than that in the semiconductor substrate, as recited in claim 6 (emphasis added).

For at least this reason, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 6.

Application No.: 10/549,291

Claim 3 was rejected under § 103(a) as being unpatentable over Iwasa in view of Shirasaki and further in view of U.S. Patent Number 4,868,632 ("Hayashi"). Claims 6, 8, and 13 were rejected under § 103(a) as being unpatentable over Iwasa in view of Shirasaki and further in view of U.S. Patent Number 6,025,628 ("Lee") and U.S. Patent Number 7,163,851 ("Abadeer"). Claim 7 was rejected under § 103(a) as being unpatentable over Iwasa in view of Shirasaki in view of Abadeer and further in view of Hayashi.

Claims 3, 6-8, and 13 variously depend from claims 1 and 6. Therefore, for at least the reasons presented above with respect to claims 1 and 6, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 3, 6-8, and 13.

New Claims

New claim 14 recites a semiconductor device that includes, among other features, a semiconductor region of a conductive type having a main surface; a trench formed in the semiconductor region and having a bottom portion; and a semiconductor FIN formed in the trench. The semiconductor device further includes source and drain regions formed so as to be buried in the trench and connected to the semiconductor FIN; a gate insulating film formed so as to cover both side surfaces of the semiconductor FIN; and a gate electrode formed on the gate insulating film and having in the trench, termination structures extending toward the bottom portion of the trench along the both sides of the semiconductor FIN. Additionally, the semiconductor device includes a heavily doped impurity region of the conductive type formed in the semiconductor region at the bottom portion of the trench and under the semiconductor FIN and the source and drain regions.

Applicants respectfully submit that the cited prior art fails to describe or suggest a

Application No.: 10/549,291

semiconductor device that includes, among other features, a semiconductor region of a conductive type having a main surface; a trench formed in the semiconductor region and having a bottom portion; a semiconductor FIN formed in the trench; source and drain regions formed so as to be buried in the trench and connected to the semiconductor FIN; and a heavily doped impurity region of the conductive type formed in the semiconductor region at the bottom portion of the trench and under the semiconductor FIN and the source and drain regions, as recited in claim 14 (emphasis added). Therefore, Applicants respectfully request consideration and allowance of claim 14.

Dependent Claims

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Because claims 1, 6, and 14 are allowable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also allowable. In addition, it is respectfully submitted that the dependent claims are allowable based on their own merits by adding novel and non-obvious features to the combination.

Based on the foregoing, it is respectfully submitted that all pending claims are patentable over the cited prior art. Therefore, it is respectfully requested that the rejection under § 103 be withdrawn.

Application No.: 10/549,291

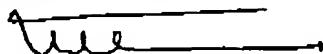
Conclusion

Having fully responded to all matters raised in the Office Action, Applicant submits that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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